

PATENT ABSTRACTS OF JAPAN

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(54) SOLID-STATE IMAGING DEVICE AND METHOD FOR DRIVING THE SAME

(57)Abstract:

PROBLEM TO BE SOLVED: To reduce the dark current in a MOS solid-state imaging device.

SOLUTION: The solid-state imaging device comprises a pixel 2 provided with a photodiode PD, a detection part N, and a transfer transistor QT by which an electric charge stored in the photodiode PD is transferred to the detection part N. The gate voltage of the transfer transistor QT at a time when the electric charge is stored in the photodiode PD is set as a negative voltage.

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CLAIMS

[Claim(s)]

[Claim 1] The solid state camera characterized by making into a negative electrical potential difference gate voltage of said transfer transistor when having the pixel equipped with the photodiode, the detecting element, and the transfer transistor that transmits the charge accumulated in said photodiode to said detecting element, and accumulating a charge in said photodiode.

[Claim 2] Said negative electrical potential difference is a solid state camera according to claim 1 characterized by considering as the electrical potential difference by which the channel section under the gate of said transfer transistor is reversed.

[Claim 3] Said negative electrical potential difference is a solid state camera according to claim 1 characterized by being less than [-0.5V].

[Claim 4] The solid state camera characterized by making into a forward electrical potential difference gate voltage of said transfer transistor when having the pixel equipped with the photodiode, the detecting element, and the transfer transistor that transmits the charge accumulated in said photodiode to said detecting element, and accumulating a charge in said photodiode.

[Claim 5] Said forward electrical potential difference is a solid state camera according to claim 4 characterized by considering as the electrical potential difference by which the channel section under the gate of said transfer transistor is reversed.

[Claim 6] Said forward electrical potential difference is a solid state camera according

to claim 4 characterized by being more than supply voltage.

[Claim 7] The solid state camera according to claim 1 or 4 characterized by forming the field which results in a semi-conductor substrate in n mold thinner than the concentration of a semi-conductor well field, or a p type semiconductor field, and consisting of directly under [of said photodiode] among said pixels.

[Claim 8] The solid state camera according to claim 1 or 4 with which the field between said photodiodes and said detecting elements is characterized by being formed in n mold thinner than the concentration of a semi-conductor well field, or a p type semiconductor field, and changing among said pixels.

[Claim 9] The solid state camera according to claim 1 or 4 characterized by forming the field which results in a semi-conductor substrate in n mold thinner than the concentration of a semi-conductor well field, or a p type semiconductor field, and consisting of directly under [of said photodiode], and the field between said photodiodes and said detecting elements among said pixels.

[Claim 10] The solid state camera characterized by having the pixel equipped with the photodiode, the detecting element, and the transfer transistor that transmits the charge accumulated in said photodiode to said detecting element, forming the overflow pass for discharging the charge which overflowed with said photodiodes in bulk other than the channel section of said transfer transistor, and changing.

[Claim 11] it forms in a field with said overflow pass from just under said photodiode to [in a field] a semi-conductor substrate -- having -- this field -- a semi-conductor -- a well -- the solid state camera according to claim 10 characterized by being formed in thin n mold or a p type semiconductor field, and consisting of the concentration of a field.

[Claim 12] said overflow pass forms in the field between said photodiodes and said detecting elements -- having -- this field -- a semi-conductor -- a well -- the solid state camera according to claim 10 characterized by being formed in thin n mold or a p type semiconductor field, and consisting of the concentration of a field.

[Claim 13] said overflow pass forms in the field from the field between just under said photodiode and said photodiode, and said detecting element to a semi-conductor substrate -- having -- this field -- a semi-conductor -- a well -- the solid state camera according to claim 10 characterized by being formed in thin n mold or a p type semiconductor field, and consisting of the concentration of a field.

[Claim 14] The actuation approach of the solid state camera which is the actuation approach of a solid state camera of having the pixel equipped with the photodiode, the detecting element, and the transfer transistor that transmits the charge accumulated in said photodiode to said detecting element, and is characterized by making gate voltage of said transfer transistor when accumulating a charge in said photodiode into a negative electrical potential difference.

[Claim 15] The actuation approach of the solid state camera according to claim 14

characterized by said negative electrical potential difference considering as the electrical potential difference by which the channel section under the gate of said transfer transistor is reversed.

[Claim 16] The actuation approach of a solid state camera according to claim 14 that said negative electrical potential difference is characterized by considering as less than [-0.5V].

[Claim 17] The actuation approach of the solid state camera according to claim 14 characterized by throwing away into a substrate side the charge which overflowed from said photodiode.

[Claim 18] The actuation approach of the solid state camera according to claim 14 characterized by pouring the charge which overflowed from said photodiode to a detecting-element side through the channel section bottom of a transfer transistor.

[Claim 19] The actuation approach of the solid state camera according to claim 14 characterized by pouring the charge which overflowed from said photodiode to the both sides by the side of a detecting element through the channel section bottom of a transfer transistor a substrate side.

[Claim 20] The actuation approach of the solid state camera which is the actuation approach of a solid state camera of having the pixel equipped with the photodiode, the detecting element, and the transfer transistor that transmits the charge accumulated in said photodiode to said detecting element, and is characterized by making gate voltage of said transfer transistor when accumulating a charge in said photodiode into a forward electrical potential difference.

[Claim 21] The actuation approach of the solid state camera according to claim 20 characterized by said forward electrical potential difference considering as the electrical potential difference by which the channel section under the gate of said transfer transistor is reversed.

[Claim 22] The actuation approach of a solid state camera according to claim 20 that said forward electrical potential difference is characterized by carrying out to more than supply voltage.

[Claim 23] The actuation approach of the solid state camera according to claim 20 characterized by throwing away into a substrate side the charge which overflowed from said photodiode.

[Claim 24] The actuation approach of the solid state camera according to claim 20 characterized by pouring the charge which overflowed from said photodiode to a detecting-element side through the channel section bottom of a transfer transistor.

[Claim 25] The actuation approach of the solid state camera according to claim 20 characterized by pouring the charge which overflowed from said photodiode to the both sides by the side of a detecting element through the channel section bottom of a transfer transistor a substrate side.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to a solid state camera especially an MOS mold solid state camera, and its actuation approach.

[0002]

[Description of the Prior Art] The MOS mold solid state camera is known as a solid state camera. Moreover, the solid state camera of the method read after transmitting the signal charge of the photodiode which constitutes a pixel among MOS mold solid state cameras to the detecting element using a transfer transistor is known. Unlike the CCD mold solid state camera, the MOS mold solid state camera of this method carries the CMOS logical circuit in the same chip, and it is constituted so that a pixel may also operate with one power source of the same low battery as a logical circuit. When a transfer transistor was an n channel MOS transistor from this, for example, the gate voltage of the transfer transistor in a pixel was binary [of 0V and supply voltage Vdd].

[0003] On the other hand, in a charge storage period, even when light does not carry out incidence to the signal charge according to the amount of incident light, two persons of the dark current component (dark electron) which flows into a photodiode are accumulated in the photodiode of a pixel. A dark electron cannot be separated with a signal charge at the time of read-out, but the dispersion serves as a noise. Especially, dispersion in the dark current for every pixel serves as a fixed pattern noise, an image grinds, and it came to have taken a photograph through glass. Moreover, time dispersion of the dark current serves as random noise. With the MOS mold solid state camera, it has been main technical problems from this how the dark current is reduced.

[0004] There is an embedding photodiode as a conventional technique for dark current reduction. The greatest source of release of the dark current is Si and SiO₂ of a photodiode upside. It is an interface, and if this depletion-izes, the dark current will flow into a photodiode. Therefore, he carbonates the oxide-film interface on the n-type-semiconductor field which constitutes the photodiode by p mold field, and is trying to suppress generating of the dark current.

[0005] Drawing 11 shows a part of pixel, i.e., the cross-section structure of an embedding photodiode and a transfer transistor, which has the conventional embedding photodiode. The pixel 70 of drawing 11, i.e., the important section, is Photodiode PD and the transfer transistor QT to the pixel field which the semi-conductor well field 72 of p mold was formed on the semi-conductor substrate 71 of n mold or p mold, and was classified by the component detached core (SiO₂ layer) 73 by the selective oxidation (LOCOS) of the p type semiconductor well field 72. It is formed and changes.

Photodiode PD forms the n-type-semiconductor field 74 used as a charge storage field in the p type semiconductor well field 72, forms the p type semiconductor field 75 of this and a reverse conductivity type in the top face of the n-type-semiconductor field 74 further, and is constituted as the so-called embedding photodiode. Transfer transistor QT The n-type-semiconductor field 74 of Photodiode PD is made into one source drain field, and the transfer gate electrode 78 is formed through gate dielectric film (for example, SiO₂ film) 77 between this field 74 and n mold source drain field 76 of another side formed in the p type semiconductor well field 72, and it is constituted. The n-type-semiconductor field 76 of another side of this transfer transistor Q is constituted as a detecting element.

[0006] In this configuration, since the p type semiconductor field 75 is formed in the interface with the oxide film 79 of n-type-semiconductor field 74 upside which constitutes Photodiode PD, depletion-ization of an interface is prevented and the dark current generated from an interface is controlled. This embeds and it is a photodiode.

[0007]

[Problem(s) to be Solved by the Invention] By the way, an MOS mold solid state camera requires low-battery actuation. For example, as for an MOS mold solid state camera, the low batteries not more than supply voltage 3V etc. are required from the supply voltage 12V grade of a CCD mold solid state camera. In this case, since a signal can be read only in the range to which the signal of a photodiode can be transmitted by the low battery, it is difficult to secure the amount of saturated signals enough. For this reason, there was a problem that it was small and gradation could not be taken, about a dynamic range.

[0008] With a low illuminance, a fixed pattern noise and random noise are seen also by the dark current component which remains with an embedding photodiode on the other hand although the dark current from the oxide-film interface of a photodiode is controlled. For this reason, the further improvement was desired in order to offer high S/N and a high sensitivity MOS mold solid state camera.

[0009] Moreover, in an MOS mold solid state camera, when the quantity of light more than saturation carries out incidence to Photodiode PD, a photoelectron overflows Photodiode PD by the signal charge by which photo electric translation was carried out, i.e., this example. This photoelectron diffuses the inside of the p type semiconductor well field 72, and breadth and the phenomenon of invading into the photodiode PD of a surrounding pixel and becoming an alias are called blooming. For blooming prevention, the runoff path (the so-called overflow pass) of a photoelectron in which it overflowed is set up beforehand, and is placed, and it prevents a photoelectron diffusing all over the p type semiconductor well field 72. Conventionally, it is the transfer transistor QT about overflow pass. It is the transfer transistor QT about the photoelectron which set it as the channel section and overflowed with Photodiodes PD. It was made to flow into a detecting-element (n mold source drain field 76) side through the channel section. In

addition, this overflowing photoelectron flows into the ** reset transistor side which is not illustrated from a detecting element.

[0010] However, by this configuration, it is the transfer transistor QT. The amount of charges which can let overflow pass if the potential of the channel section becomes about 0.5-0.6V and potential of this channel section is made low at the 0V side when 0V are given to the transfer gate electrode 78 when potential of the channel section was made low namely, becomes small. In an MOS mold solid state camera, there was a request of wanting to want to take the large amplitude of the gate voltage which impresses the amount of saturated signals to the transfer gate in order to carry out and to take a large dynamic range, an increase and, namely, to make low potential of the channel section of the transfer transistor in a charge storage period. However, in the conventional MOS mold solid state camera, there was a problem that it was incompatible the increase of the amount of saturated signals, to carry out and to enlarge a dynamic range, and to secure the capacity of above-mentioned overflow pass.

[0011] Although **** explained the case where an n channel MOS transistor was used for a transfer transistor by using a signal charge as an electron, also when the p channel MOS transistor of a reverse conductivity type is used for a transfer transistor by making a signal charge into a hole, the same technical problem arises.

[0012] This invention offers the solid state camera which enabled further reduction of the dark current, and its actuation approach in view of an above-mentioned point. This invention is combined and the solid state camera which secures the function of overflow pass and enabled it to control a blooming more certainly, and its actuation approach are offered.

[0013]

[Means for Solving the Problem] This inventions are the solid state camera equipped with the photodiode, the detecting element, and the transfer transistor that transmits the charge accumulated in the photodiode to a detecting element, and its actuation approach, and make gate voltage of the transfer transistor when accumulating an electron or a hole in a photodiode as a charge a negative electrical potential difference or a forward electrical potential difference. This invention pours the charge with which it overflowed from the photodiode through the inside of bulk other than the channel section of a transfer transistor. The field which pours the charge with which it overflowed from the photodiode is formed in the field of concentration thinner than the concentration of a semi-conductor well field.

[0014] In this invention, by making gate voltage of the transfer transistor when accumulating an electron or a hole in a photodiode as a charge into a negative electrical potential difference or a forward electrical potential difference, the channel section of a transfer transistor is reversed and generating of the dark current component from the interface of the channel section and gate dielectric film is controlled. By pouring the charge with which it overflowed from the photodiode through the inside of bulk other

than the channel section of a transfer transistor, the so-called overflow pass area becomes large, and the function as overflow pass goes up.

[0015]

[Embodiment of the Invention] There are various opinions about sources of release of the dark current component which remains other than the dark current generated from the interface of a photodiode top face and an insulator layer. For example, they are the opinion that the minority carrier of the opinion to which it is supposed that the dark current from the oxide-film interface of the photodiode upper part is not suppressed enough, the opinion it is supposed that the edge of the LOCOS (selective oxidation) insulating layer which is a component detached core has a defect, and have been become the source of release of the dark current, a p type semiconductor well field, or a p type semiconductor substrate flows by diffusion, the opinion it is supposed that are based on thermal generating by the depletion layer between a photodiode and a p type semiconductor well field.

[0016] On the other hand, this invention persons clarified the following point, as a result of analyzing the dark current component which remains carefully.

(1) To an embedding photodiode, the dark current from the insulator layer (for example, gate oxide) interface under the transfer gate is dominant. As the arrow heads a and b of drawing 10 (it is the same configuration as drawing 11) show, the dark current generated in the insulator layer interface under the transfer gate according to the defect 81 of an interface divides and flows into the n-type-semiconductor field 74 of Photodiode PD, and n mold source drain field 76 used as a detecting element.

(2) Even if the insulator layer interface under the transfer gate forms p type layer in extent which can transmit the signal charge of a photodiode by the low battery not more than 3.3V thinly, the effectiveness of dark current reduction is small.

(3) Most residual dark currents can be reduced by making the transfer gate into a negative electrical potential difference during an are recording period, and forming the channel of an electron hole in the oxide film interface under the transfer gate. By this, S/N can improve dramatically and can improve image quality by leaps and bounds.

[0017] Since the amount of saturation charges of a photodiode increases, the gradation of raising and drawing can be made to increase a dynamic range by considering as the configuration of the above (3). If a reason makes negative potential the low of the gate voltage impressed to the transfer gate and a high level is not changed, it is because the amplitude of the part transfer gate increases. The effectiveness whose amount of saturation charges of this increases needs to be acquired by making the transfer gate into negative potential, and that negative potential does not need to be the level which generates the channel of an electron hole.

[0018] As overflow pass for on the other hand discharging the charge which overflowed with photodiodes, it is desirable to form in bulk other than the channel section of a transfer transistor. That is, a semi-conductor well field is not formed in the field of the

predetermined direction of the perimeter of a photodiode, but n mold or the p type semiconductor field of high impurity concentration thinner than the high impurity concentration of a semi-conductor well field is instead formed in it, and they are n- with this thin high impurity concentration, or p. - The charge with which it passed [or] the substrate side by having considered the semiconductor region as overflow pass, passed the detecting-element side, or overflowed to both is discharged.

[0019] By this configuration, overflow pass can set it as the bulk part with the large cross-sectional area instead of the narrow channel section. Since overflow pass can be set widely, blooming suppression capacity can set up the potential of a large thing, therefore overflow pass lowness, can increase the amount of saturated signals of a photodiode, and can enlarge a dynamic range. Since the function as overflow pass of the channel section falls substantially in the case of the conventional example especially when impressing negative potential to the transfer gate, this invention structure is effective.

[0020] Hereafter, the gestalt of operation of this invention is explained with reference to a drawing.

[0021] Drawing 1 shows the gestalt of 1 operation of the solid state camera of this invention, i.e., an MOS mold solid state camera. The MOS mold solid state camera 1 concerning the gestalt of this operation has the sensor section 3 by which two or more pixels 2 [211, 212, 221, 222] were arranged in the shape of a matrix, the vertical-scanning circuit 4 and the horizontal scanning circuit 5 which drives the sensor section 3, the CDS (correlation duplex sampling) / signal holding circuit 6 [61 and 62 ..] which receives the signal of the pixel 2 for a party of the sensor section 3, and the output amplifier 7, and changes. In this example, although the pixel 2 is drawn by the 2 piece x2 piece for convenience, it is arranged much actually.

[0022] The photodiode PD with which the configuration of each pixel 2 performs photo electric translation [PD11, PD12, PD21, PD22] Transfer transistor QT which transmits the signal charge of Photodiode PD to a detecting element N [N11, N12, N21, N22] (MOS transistor) [QT11, QT12, QT21, and QT22], Magnification transistor QA which outputs the potential of a detecting element N to the vertical signal line 8 (MOS transistor) [QA11, QA12, QA21, and QA22], The address transistor (MOS transistor) [QD11, QD12, QD21, and QD22] QD which chooses the line of a pixel 2, Reset transistor QR which resets the potential of a detecting element N (MOS transistor) It consists of [QR11, QR12, QR21, and QR22].

[0023] For Photodiode PD, the cathode is the transfer transistor QT. It connects with one main electrode and the anode is grounded. Transfer transistor QT The main electrode of another side is the magnification transistor QA. While connecting with a gate electrode, it is the reset transistor QR. It connects with one main electrode. Transfer transistor QT A gate electrode is connected to the vertical sense line 11 from the vertical-scanning circuit 4. Magnification transistor QA The main electrode of one of

these is connected to supply voltage Vdd, and the main electrode of another side is the address transistor QD. It minds and connects with the vertical signal line 8. Address transistor QD A gate electrode is connected to the vertical selection line 12 from the vertical-scanning circuit 4. Reset transistor QR The main electrode of the another side is connected to supply voltage Vdd, and the gate electrode is connected to the reset line 13 from the vertical-scanning circuit 4.

[0024] The buffer circuit where 15 was connected to the vertical selection line 12, and 16 show the buffer circuit connected to the reset line 13. These buffer circuits 15 and 16 are constituted by the inverter circuit with the so-called CMOS transistor formed with the p channel MOS transistor 23 and the n channel MOS transistor 24 as shown in drawing 3. The drain side of the p channel MOS transistor 23 is connected to supply voltage Vdd, and the source side of the n channel transistor 24 is connected to a gland (GND). Moreover, the input side of this inverter circuit is connected to the vertical-scanning circuit 4, and an output side is connected to the vertical selection line 12 or the reset line 13. Although buffer circuits 15 and 16 were constituted from one step of inverter circuit by this example, respectively in order to make an understanding easy, it can constitute from two or more steps of inverter circuits.

[0025] In these buffer circuits 15 and 16, when the p channel MOS transistor 23 turns on, supply voltage Vdd is outputted to the vertical selection line 12 or the reset line 13 of an output side, when the low of a pulse is inputted from the vertical-scanning circuit 4 side, and the high level of a pulse is inputted, the n channel MOS transistor 24 turns on and a negative electrical potential difference is outputted to the vertical selection line 12 or the reset line 13 of an output side.

[0026] Each vertical signal line 8 is the load transistor (MOS transistor) QL which makes the duty of a constant current source at the end. It connects and is a switching device (MOS transistor) QS to the other end. It minds and CDS / signal holding circuit 6 is connected. Incidentally, CDS / signal holding circuit 6 is circuits which output the difference of two voltage signals inputted by time series. in addition, load transistor QL the gate -- of operation pulse phiL it impresses -- having -- switching device QS **** -- of operation pulse phiSH is impressed.

[0027] The outgoing end of CDS / signal holding circuit 6 is the level switching device (MOS transistor) QH. It minds and connects with the level signal line 9. Level switching device QH Horizontal scanning pulse phiH from the horizontal scanning circuit 5 impressed to the gate It is controlled by [phiH1, phiH2, ...].

[0028] Furthermore, at the gestalt of this operation, it is the transfer transistor QT during a charge storage period. In the means and this example which impress a negative electrical potential difference to a gate electrode, the negative electrical-potential-difference generation circuit 21 is formed. The negative electrical-potential-difference generation circuit 21 can be seen from a well-known booster circuit and the so-called supply voltage, and the circuit which carries out

pressure up of the grand (GND) electrical potential difference to a negative side can be used. The output of the negative electrical-potential-difference generation circuit 21 is inputted into the buffer circuit 31 connected to the vertical-scanning circuit 4.

[0029] A buffer circuit 31 is constituted by the inverter circuit with the so-called CMOS transistor formed with the p channel MOS transistor 33 and the n channel MOS transistor 34 as shown in drawing 4. And supply voltage Vdd is connected to the drain side of the p channel MOS transistor 33, and the negative electrical-potential-difference generation circuit 21 is connected to the source side of the n channel transistor 34. Moreover, the input edge of this inverter circuit is connected to the vertical-scanning circuit 4, and an outgoing end is connected to the vertical sense line 11. Although the buffer circuit 31 was constituted from one step of inverter circuit by this example in order to make an understanding easy, it can constitute from two or more steps of inverter circuits.

[0030] A buffer circuit 31 is separated and formed of the semi-conductor well field 36, as drawing 1 shows. In more detail, as shown in drawing 4, the p channel MOS transistor 33 is formed in the n-type-semiconductor well field 37, and the n channel MOS transistor 34 is formed in the p type semiconductor well field 38. Therefore, the output of the negative electrical-potential-difference generation circuit 21 goes into the p type semiconductor well field 38 of a buffer circuit 31, and the source field of n-type channel MOS transistor 34 in this p type semiconductor well field 38. The threshold of the n channel MOS transistor 34 is set up highly.

[0031] In this buffer circuit, therefore an inverter circuit 31, when the p channel MOS transistor 33 turns on, supply voltage Vdd is outputted to the vertical sense line 11 of an output side, when the low of a pulse is inputted from the vertical-scanning circuit 4 side, and the high level of a pulse is inputted, the n channel MOS transistor 34 turns on and a negative electrical potential difference is outputted to the vertical sense line 11 of an output side.

[0032] Next, actuation of the MOS mold solid state camera 1 mentioned above is explained using the timing of drawing 2 of operation. Here, supply voltage Vdd is set to 3.0V, and the output of the negative electrical-potential-difference generation circuit 21 is set to -1.1V. Moreover, its attention is paid to the pixel 211 at the lower left of drawing 1. First, it is load MOS transistor QL at the time (during the so-called charge storage period) of a pixel un-choosing [of the 1st line] containing a pixel 211. Of operation pulse phiL impressed to the gate of [QL1, QL2], the read pulse phiT1 supplied to the vertical sense line 11, the selection pulse phiA1 supplied to the vertical signal line 12, and reset line 131 The reset pulse phiR1 supplied is a low. Here, only in a read pulse phiT1, in response to the fact that the output of the negative electrical-potential-difference generation circuit 21, a low becomes negative potential, -1.1V [for example,]. Other phiL, phiA1, and phiR1 are set to 0V. The potential of a detecting element N11 serves as a value a little lower than supply voltage 3.0V, and is

the vertical signal line 81. Potential Vsig1 is set to 0V. By this, they are the transfer transistor QT11, the address transistor QD11, and the reset transistor QR11. It will be in both OFF states and a signal charge is accumulated in a photodiode PD 11. The so-called photoelectron recording is performed in this example.

[0033] Next, of operation pulse phiL The selection pulse phiA1 is made into a high level, and it is load MOS transistor QL. Address transistor QD of the 1st line ** is made into an ON state. At this time, it is load MOS transistor QL (since load transistor QL1) and the magnification transistor QA of the 1st line (the view pixel 211 the magnification transistor QA 11) construct a source follower circuit in the view pixel 211, in the vertical signal line 81, the electrical potential difference corresponding to the potential of a detecting element N11 appears.).

[0034] Next, reset transistor QR A reset pulse phiR1 (high level) is impressed to the gate. At this time, the dark charge (this example dark electron) accumulated in the detecting element N11 sweeps, and is thrown away, a detecting element N11 is reset by supply voltage Vdd, and it is the vertical signal line 81. It becomes the value to which potential also corresponds.

[0035] Next, vertical signal line 81 They are CDS / signal holding circuit 61, using potential as reset level. It inputs. Next, vertical sense line 111 It leads and is the transfer transistor QT of the 1st line. A read pulse (high level) is impressed. At this time, it is the transfer transistor QT of the 1st line. It is turned on and the signal charge and dark charge of a photodiode PD 11 are the transfer transistor QT11. It lets it pass and is transmitted to a detecting element N11. The potential of a detecting element N11 corresponds and falls in connection with this. Load MOS transistor QL1 and magnification transistor QA 11 By the source follower circuit to depend, it is the vertical signal line 81. Potential also changes by the charge of the sum total of a signal charge and a dark charge.

[0036] This vertical signal line 81 It lets a switching device QS1 pass by making potential into signal level, and they are CDS / signal holding circuit 61. It inputs, and difference with previous reset level is taken and held.

[0037] Next, reset transistor QR Reset line 131 It lets it pass, a reset pulse phiR1 (high level) is impressed, and the reset transistor QR (the view pixel 211 reset transistor QR11) is made into an ON state. A detecting element N11 is reset by supply voltage, and it is the vertical signal line 81. It is reset by the potential to which potential is also equivalent. The selection pulse phiA1 is returned to a low (0V). Since a source follower circuit is turned off, the pixel of the line returns to the condition of not choosing, and a charge storage begins. Vertical signal line 81 It returns to 0V.

[0038] Henceforth, a charge storage period comes until the line of the following pixel is chosen. By the above actuation, all the pixels including pixels other than view pixel 211 of the 1st line drive to coincidence, and the signal for one line (namely, signal of the difference of signal level and reset level) is memorized simultaneously in CDS / signal

holding circuit 6 [61 and 62].

[0039] Then, although not described to drawing 2, the horizontal scanning circuit 5 is driven, and it is horizontal scanning pulse phiH. Level switching device QH It is impressed by [QH1, QH2], the signal of the pixel for one line held in CDS / signal holding circuit 6 is led to the level signal line 9 in order, and it lets the output amplifier 7 pass, and is an output terminal tOUT. It outputs.

[0040] If same actuation is performed about the pixel of the 2nd line as follows, when reading appearance of the signal of the 2nd line is carried out and it carries out sequential actuation of the vertical-scanning circuit 4, the signal of the pixel of all lines can be read.

[0041] An important thing is the transfer transistor QT to a charge storage period at the gestalt of this operation. It is that transfer gate potential is negative potential. If this transfer gate potential turns into negative potential, since the amplitude of transfer gate voltage will increase, the amount of saturated signals increases, and a dynamic range is expanded. Another important point is that the value of the negative potential of the transfer gate is the level (here -1.1 V) by which a channel (this example channel of an electron hole) is formed in the bottom of the gate. Although the dark current flowed into Photodiode PD at the charge and coincidence by which photo electric translation was carried out to the charge storage period, the source of release of the dark currents main to an interface with an oxide film, when the charge storage field (for example, n-type-semiconductor field) of a photodiode uses the so-called embedding photodiode in which the field (for example, p type semiconductor field) of a reverse conductivity type was formed was an oxide-film interface under the transfer gate as a photodiode PD, as mentioned above. The dark current can be prevented by forming the channel of an electron hole here by making the transfer gate into negative potential, without degrading a transmission characteristic.

[0042] Drawing 9 is property drawing of the dark current of a pixel to the negative electrical potential difference impressed to the transfer gate electrode of the transfer transistor PD. An axis of abscissa shows negative potential [low of gate voltage] (V) of the transfer gate, and an axis of ordinate shows the relative value of a dark current component, respectively. The circuitry of a pixel was the same and measured measurement about two kinds of pixels from which a layout differs. O As for both two samples, \diamond marks, and $**$ marks of the 1st layout (the same pixel), the mark and x mark show two samples of the 2nd layout (the same pixel). [both] From property drawing of drawing 9, the layout of a pixel is not related and it is admitted by giving a negative electrical potential difference to the transfer gate at a charge storage period that the dark current decreases. And reduction of the dark current arises from about -0.5V, negative potential is or less about -0.8V, and the abbreviation dark current is set to 0. as the negative potential given to the transfer gate with the gestalt of this operation -0.5 -- it can take preferably or less for -0.8 V or less.

[0043] Drawing 5 - drawing 8 are the pixel applied to this invention, respectively especially its photodiode PD, and the transfer transistor QT. The gestalt of operation of a component is shown.

[0044] The gestalt of operation shown in drawing 5 is Photodiode PD and the transfer transistor QT to the pixel field which the semi-conductor well field 42 of the 2nd conductivity type, for example, p mold, was formed on the semi-conductor substrate 41 of n mold or p mold, and was divided by the component detached core (SiO₂ layer) 43 by the selective oxidation (LOCOS) of the p type semiconductor well field 42. It is formed and changes. Photodiode PD forms the n-type-semiconductor field 44 of the 1st conductivity type used as a charge storage field in the p type semiconductor well field 42, forms the p type semiconductor field 45 in the front face of the n-type-semiconductor field 44 further at this and a reverse conductivity type, and is constituted as the so-called embedding photodiode. Transfer transistor QT The n-type-semiconductor field 44 of Photodiode PD is made into one source drain field, and the transfer gate electrode 48 is formed through gate dielectric film (for example, SiO film) 47 between this field 44 and the source drain field 46 of another side formed in the p type semiconductor well field 42, and it is constituted. This transfer transistor QT The n-type-semiconductor field 46 of another side is constituted as a detecting element N. In this configuration, although a crystal defect 40 arises in an interface with the insulator layer (for example, oxide film) 50 of the photodiode PD upper part, and the gate-dielectric-film interface under the transfer gate, generating of the dark current from the oxide-film interface of Photodiode PD is prevented by the p type semiconductor field 45 of the embedding photodiode PD. On the other hand, generating of the dark current from a transfer gate lower-bound side is prevented by making potential of the transfer gate electrode 48 into negative potential, -1.1V [for example,], and forming an inversion layer 49, i.e., the channel section of an electron hole, in the bottom of the gate electrode 48.

[0045] The gestalt of operation shown in drawing 6 is n of concentration thinner than the high impurity concentration of the p type semiconductor well field 42 so that high impurity concentration may reach directly under [n-type-semiconductor field 44] Photodiode PD in the configuration of drawing 5 even at the semi-conductor substrate 51 rather than n mold or the p type semiconductor well field 42, using the semi-conductor substrate 51 of p mold of thin concentration as a semi-conductor substrate. - A field or p - The semiconductor region 52 by the field is formed and it is constituted. Other configurations give the same sign to the part which corresponds since it is the same as that of drawing 5 , and omit duplication explanation.

[0046] In this configuration, generating of the dark current from the oxide-film interface of Photodiode PD and the dark current from a transfer gate lower-bound side is prevented by the same configuration as drawing 5 . Furthermore, they are n-field of low concentration [instead of / field / 42 / p type semiconductor well], or p, without

forming the p type semiconductor well field 42 in the semi-conductor substrate 51 only directly under photodiode PD using a low-concentration p type semiconductor substrate from a n-type-semiconductor substrate or the p type semiconductor well field 42. - Since the semiconductor region 52 by the field is formed and it is constituted, as the overflow pass of a charge shows an arrow head c, it can set to the semi-conductor substrate 51 from Photodiode PD in a lengthwise direction. Therefore, since overflow pass area can be set up widely, an overflow pass function improves and blooming suppression capacity becomes large. for this reason -- since the potential of overflow pass (semiconductor region 52) can be set up lowness -- the increase of the amount of saturated signals of Photodiode PD -- it can carry out and a dynamic range can be enlarged. Although this overflow path structure is useful regardless of transfer gate negative potential, if it uses together with transfer gate negative potential, since it can substitute for the capacity as overflow pass of the channel section being weak, especially effectiveness becomes large.

[0047] The gestalt of operation shown in drawing 7 is the transfer transistor QT which serves as a detecting element N from directly under [photodiode PD] in the configuration of drawing 5 . n of the concentration thinner than the high impurity concentration of the p type semiconductor well field 42 into the part which reaches the source drain field 46 - The semiconductor region 54 by the field or p-field is formed, and it is constituted. At least, it is n of thin concentration about the field between the source drain fields 46 used as Photodiode PD and a detecting element N. - A field or p - It forms in the semiconductor region 54 by the field. Other configurations give the same sign to the part which corresponds since it is the same as that of drawing 5 , and omit duplication explanation. In this configuration, generating of the dark current from the oxide-film interface of Photodiode PD and the dark current from a transfer gate lower-bound side is prevented by the same configuration as drawing 5 . Into furthermore, the part applied to the source drain field 46 of a detecting element N from Photodiode PD It is n of concentration thinner than the high impurity concentration of the p type semiconductor well field 42 instead, without forming the p type semiconductor well field 42. - Field, Or p - Since the semiconductor region 54 by the field was formed, and overflow pass is set towards a detecting element N through under surface than the channel section as shown in an arrow head d the potential of that blooming suppression capacity becomes [overflow pass area] large greatly like drawing 6 , and overflow pass (semiconductor region 54) -- slight lowness -- it can set up -- the increase of the amount of saturated signals of Photodiode PD -- it can carry out and a dynamic range can be enlarged.

[0048] The gestalt of operation of drawing 8 is the configuration which combined the configuration of drawing 6 and drawing 7 . That is, it is n of concentration thinner than the high impurity concentration of the p type semiconductor well field 42 so that it may reach directly under the part applied from under the n-type-semiconductor field 44 of

PD to a part of channel subordinate and n mold source drain field in drawing 5 at the semi-conductor substrate 51. - A field or p - The semiconductor region 56 by the field is formed and it is constituted. Other configurations give the same sign to the part which corresponds since it is the same as that of drawing 5, and omit duplication explanation. In this configuration, as overflow pass shows arrow heads c and d, it is formed so that it may go to a substrate 41 and detecting-element N side, and the same effectiveness as above-mentioned drawing 6 is acquired.

[0049] n of the thin concentration of drawing 6 - drawing 8 - A field or p - Especially the semiconductor regions 52 and 5456 by the field cannot be formed, but substrate high impurity concentration can be used for them as it is.

[0050] It is the transfer transistor QT during the charge storage period which accumulates a charge in Photodiode PD according to the MOS mold solid state camera 1 concerning the gestalt of this operation mentioned above. By impressing a negative electrical potential difference to the gate electrode 48, the dark current component generated under the transfer gate is controlled, and the dark current in a solid state camera can be reduced. Consequently, S/N can improve and image quality can be improved. The reduction of this dark current itself contributes to improvement in a dynamic range. By impressing a negative electrical potential difference to the gate electrode 48, it can become possible to enlarge the amplitude of gate voltage, it can make [many] it, the amount of saturated signals, i.e., the saturation electron number, of Photodiode PD, and can open a dynamic range. n- A field or p - The semiconductor regions 52 and 54 which consist of fields, or 56 is formed, and it is the transfer transistor QT about overflow pass. Since it forms in bulk other than the channel section, a large overflow pass area can be taken and the function as overflow pass goes up it substantially. Therefore, control of a blooming becomes good. Moreover, control of a blooming and amplification of a dynamic range can be reconciled.

[0051] Although considered as the configuration which built the negative electrical-potential-difference generation circuit 21 in the transfer gate as a means to input a negative electrical potential difference in above-mentioned drawing 1, it is good also as a configuration which draws a volt input terminal independently and inputs a negative electrical potential difference from the solid state camera exterior. At drawing 1 of the example of a top, they are Photodiode PD, four MOS transistors QT, QA, QD, and QL about a pixel 2. Although constituted, they are a photodiode and the transfer transistor QT at least. If it is the configuration to include, this invention is applicable even if it is the pixel of other configurations.

[0052] In the example of a top, although it is the case where a signal charge is applied to the MOS mold solid state camera used as the electron, a signal charge is applicable also to the MOS mold solid state camera made into the hole. In this case, with ****, as for a transfer transistor, the p channel MOS transistor of a reverse conductivity type is used. Therefore, when accumulating a charge in a photodiode, it makes as [impress / the

forward electrical potential difference which carried out pressure up as gate voltage of the transfer transistor of a p channel more than the forward electrical potential difference, i.e., supply voltage,]. The configuration of a pixel can be considered as the configuration which transposed each substrate and the conductivity type of a semiconductor region to the reverse conductivity type in drawing 5 mentioned above - drawing 8. Overflow pass can be formed similarly.

[0053]

[Effect of the Invention] According to the solid state camera concerning this invention, by constituting so that gate voltage of the transfer transistor when accumulating an electron or a hole in a photodiode as a charge may be made into a negative electrical potential difference or a forward electrical potential difference, the dark current can be decreased sharply, S/N can be improved and image quality can be improved. By using a negative electrical potential difference or a forward electrical potential difference, the large amplitude of the transfer gate can be taken, the amount of saturated signals of a photodiode can be enlarged, and a dynamic range can be expanded. The reduction of the dark current itself leads to improvement in a dynamic range.

[0054] By forming the field section which leads in bulk other than the channel section of a transfer transistor to a substrate, detecting-element or substrate, and detecting-element side in n mold thinner than the concentration of a semi-conductor well field, or a p type semiconductor field so that it may become overflow pass, the overflow pass cross-sectional area can be set up widely, the function of overflow pass can be raised, and a blooming can fully be controlled. Moreover, it is compatible with amplification of a dynamic range.

[0055] According to the actuation approach of the solid state camera concerning this invention, by making gate voltage of the transfer transistor when accumulating an electron or a hole in a photodiode as a charge into a negative electrical potential difference or a forward electrical potential difference, the dark current can be made to be able to decrease sharply and improvement in S/N of a solid state camera and improvement in image quality can be aimed at. Moreover, since the large amplitude of the transfer gate can be taken, the amount of saturated signals of a photodiode is increased and amplification of a dynamic range can be aimed at. It becomes possible to fully control a blooming by letting the inside of bulk other than the channel section of a transfer transistor pass, and pouring the charge which overflowed from the photodiode to a substrate, detection or substrate, and detection side. Coexistence with a dynamic range is also attained.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the block diagram showing the gestalt of 1 operation of the solid state camera of this invention.

[Drawing 2] It is the timing chart of operation with which explanation of the solid state camera of Drawing 1 of operation is presented.

[Drawing 3] It is the circuit diagram showing the example of the buffer circuit of 1 applied to this invention.

[Drawing 4] It is the circuit diagram showing the example of other buffer circuits applied to this invention.

[Drawing 5] It is the sectional view showing the gestalt of 1 operation of the component of the photodiode which constitutes the pixel applied to this invention, and a transfer transistor.

[Drawing 6] It is the sectional view showing the gestalt of other operations of the component of the photodiode which constitutes the pixel applied to this invention, and a transfer transistor.

[Drawing 7] It is the sectional view showing the gestalt of other operations of the component of the photodiode which constitutes the pixel applied to this invention, and a transfer transistor.

[Drawing 8] It is the sectional view showing the gestalt of other operations of the component of the photodiode which constitutes the pixel applied to this invention, and a transfer transistor.

[Drawing 9] It is property drawing showing the negative potential of the transfer gate and the relation of the dark current of a pixel with which explanation of this invention is presented.

[Drawing 10] It is the sectional view with which explanation of generating of the dark current is presented.

[Drawing 11] It is the sectional view showing the component of the photodiode which constitutes the pixel of the conventional MOS mold solid state camera, and a transfer transistor.

[Description of Notations]

1 [... Vertical-scanning circuit,] ... A solid state camera, 2 ... A pixel, 3 ... The sensor section, 4 5 ... A horizontal scanning circuit, 6 ... CDS / signal holding circuit, 21 ... Negative electrical-potential-difference generation circuit, PD ... A photodiode and QT ... A transfer transistor, QA ... Magnification transistor, QD ... An address transistor, QR, a reset transistor, QL ... A load transistor and QS ... A switching device, QH ... Level switching device, 41 ... A semi-conductor substrate, 42 ... A semi-conductor well field, 43 ... Component detached core, 44 [... A gate insulating layer, 48 / ... A gate electrode, 52 54, 56 / ... Semiconductor region (overflow pass)] ... A n-type-semiconductor field, 45 ... A p type semiconductor field, 46 ... A source drain field (detecting element), 47